METAL OXIDE SEMICONDUCTOR HETEROSTRUCTURE FIELD EFFECT TRANSISTOR

REFERENCE TO PRIOR APPLICATION

The current application claims priority to co-pending provisional application serial number 60/235,563, filed on 09/27/2000.

BACKGROUND OF THE INVENTION

1. FIELD OF THE INVENTION

The current invention relates generally to the production of nitride based heterostructure devices. In particular, the present invention generally relates to nitride based heterostructures having a silicon dioxide layer for controlling the reverse leakage of current.

2. BACKGROUND ART

Gallium-Nitride (GaN) based Metal Semiconductor Metal (MSM) devices for visible-blind ultraviolet detection may have reverse leakage current values of about 1×10^{-5} A-cm^{-2} (at -5 V) for interlaced electrode geometry MSM detectors. While GaN based transparent Schottky barrier detectors have a very sharp visible-blind cutoff and responsivity values as high as about 0.18 A/W, these devices have reverse leakage currents of approximately 1×10^{-6} A-cm^{-2}.

Additionally, AlGaN/GaN Heterostructure Field Effect Transistors (HFETs) may have applications in microwave and optical communication

systems. GaN-based Metal Insulator Field Effect Transistors (MISFETs) using i-GaN, i-AlGaN/GaN and Si_3N_4 as the gate insulator have been attempted. While these devices were operational, they exhibited a current-voltage characteristic collapse at high drain biases due to a large density of interface states. GaN-based Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) using Ga_2O_3 and Gd_2O_3 oxides for the gate insulator have also been created. However, these devices exhibited a much smaller transconductance than conventional GaN-based High Electron Mobility Transistors.

Therefore, there exists a need for nitride based semiconductor devices having substantially lower reverse leakage currents and performance characteristics comparable or better than conventional devices in all other respects.

BRIEF SUMMARY OF THE INVENTION

The current invention provides a method and structure for controlling reverse current leakage in semiconductor devices by providing nitride based heterostructures having a silicon dioxide dielectric layer.

In a first aspect of the present invention, a method of producing nitride based heterostructure devices is provided. The method comprises the steps of: providing a substrate; applying a first layer over the substrate wherein the first layer includes nitrogen; and applying a dielectric layer over the first layer wherein the dielectric layer includes silicon dioxide.

In a second aspect of the present invention, a method of producing nitride based heterostructure devices is provided. The method comprises the steps of: providing a substrate; applying a first layer over the substrate wherein the first layer includes gallium and nitrogen; and applying a dielectric layer over the first layer wherein the dielectric layer includes silicon dioxide.

In a third aspect of the present invention, a nitride based heterostructure device is provided. The device comprises: a substrate; a first layer over the substrate wherein the first layer includes nitrogen; and a dielectric layer over the first layer wherein the dielectric layer includes silicon dioxide.

The exemplary aspects of the present invention are designed to solve the problems herein described and other problems not discussed, which are discoverable by a skilled artisan.

BRIEF DESCRIPTION OF THE DRAWINGS

These and other features and advantages of this invention will be more readily understood from the following detailed description of the various aspects of the invention taken in conjunction with the accompanying drawings in which:

Fig. 1 shows the typical dark I-V characteristics of an approximately 400 μm diameter Schottky diode;

Fig. 2 shows dark and light I-V curves for an approximately 200 μm diameter lateral Schottky photodiode;

Fig. 3 shows the schematic of an AlGaN/GaN MOSFET structure;

Fig. 4 shows the measured C-V curves of a base-line AlGaN/GaN HFET and of a GaN/AlGaN-based MOSFET;

Fig. 5a shows the measured I-V characteristics of a base-line AlGaN/GaN HFET;

Fig. 5b shows the measured I-V characteristics of a GaN/AlGaN-based MOSFET;

Fig. 6a shows the device saturation current in the saturation region for the MOSFETs and base-line HFETs;

Fig. 6b shows the transconductance in the saturation region for the MOSFETs and base-line HFETs;

Fig. 7 shows the gate leakage current for a MOSFET and a base-line HFET with identical device geometries;

Fig. 8 shows the MOSFET gate current versus temperature;

Fig. 9 is a Second Electron emission Microscopy (SEM) image depicting the multi gate (MG) Metal-Oxide-Semiconductor Heterostructure Field Effect Transistor (MOSHFET) design;

Fig. 10 shows the current (pulsed and DC) versus total gate width measurements for MOSHFETs and base-line HFETs;

Fig. 11 shows the I-V characteristics of an MG MOSHFET switch; and

Fig. 12 shows the breakdown voltage for both MOSHFETs and base-line HFETs as a function of gate-to-drain separation.

It is noted that the drawings of the invention are not to scale. The drawings are intended to depict only typical embodiments of the invention, and

therefore should not be considered as limiting the scope of the invention. In the drawings, like numbering represents like elements between the drawings.

DETAILED DESCRIPTION OF THE INVENTION

It is understood that for the purposes of the present invention, Al means Aluminum, In means Indium, Ga means Gallium, N means Nitrogen, Si means Silicon, O means Oxygen, Ti means Titanium, Ni means Nickel, Pt means Platinum and Au means Gold.

Methods and structures are presented herein that suppress the leakage current found in many GaN-based devices. One way to suppress the leakage current is to use a dielectric layer. The SiO_2/GaN heterointerface provides high quality and leads to the passivation of the surface states. The selection of the lateral geometry precludes the need for mesa etching and, hence, significantly reduces the reverse leakage. The leakage current is further reduced by surface passivation of the devices using a Plasma Enhanced Chemical Vapor Deposited (PECVD) SiO_2 layer.

In one embodiment of the current invention, a basal plane sapphire substrate was provided. In the next step, an approximately 800 Å thick AlN buffer layer was grown at about 600° C and 76 Torr over the basal plane sapphire substrate. After this, an epilayer was applied. The epilayer structure for the device consisted of a roughly 1.2 μm thick active layer of n^--GaN, which was deposited at about 1000° C and 76 Torr using a low pressure Metal Organic

Chemical Vapor Deposition (MOCVD). The room temperature carrier density for the active n-GaN layer was about 3 x $10^{16}cm^{-3}$. Finally, a dielectric layer was added over part of the wafer. This layer included a roughly 0.1 µm thick layer of SiO_2 which was deposited onto a part of the wafer surface using PECVD while the other part of the wafer remained uncovered.

The device further comprised lateral geometry transparent Schottky barriers surrounded by annular Ohmic contacts. The Schottky barriers were formed both in the SiO_2 covered and the non-SiO_2 regions. The Ohmic contacts were formed using Ti/Al/Ni/Au and were annealed at about 650° C for 1 minute in a forming gas. The transparent Schottky barriers were formed with an approximately 50-75 Å thick Pt layer, which was deposited using e-beam metallization and a standard liftoff process. Schottky barriers with diameters ranging from about 50 to 400 mm were fabricated. The Ohmic contact and the transparent Schottky barriers were separated by about a 10 µm gap.

It should be recognized that other nitrogen-based binary compounds including one element from the group-III element group, ternary compounds including two elements from the group-III element group, and quaternary compounds including three elements from the group-III element group are suitable for use in the active layer. The active layer may also comprise multiple layers of the above-described binary, ternary and/or quaternary compounds. The chemical compositions of the layers may be substantially constant, abruptly change or gradually change over distance within layers or from layer to layer. Additionally, while SiC and sapphire are used as the substrates throughout the

examples, it should be recognized that the current invention applies equally to the use of other substrates including sapphire, SiC, spinel substrates and silicon.

The product of this and other embodiments of the current invention can be used in many types of semiconductor devices, power switching devices and microwave devices. These devices include, for example, photodetectors, field effect transistors, gated bipolar junction transistors, gated hot electron transistors, gated heterostructure bipolar junction transistors, gas sensors, liquid sensors, pressure sensors and multi function sensors of pressure and temperature.

Turning to Figure 1, current versus voltage is plotted for the dark I-V characteristics of an approximately 400 μm diameter Schottky diode with SiO_2 passivation (solid curve) and without SiO_2 passivation (dashed curve). Both devices were fabricated on the same wafer. As seen in Figure 1, for the voltage range of about -10 to -20 V, the leakage current of the device with SiO_2 passivation 10 was about 100 - 10,000 times less than that of the device without passivation 12.

In Figure 2, current versus voltage is plotted for the dark and light characteristics of an approximately 200 μm diameter SiO_2 passivated Schottky diode. As seen, the dark current is about 1 pA at five volts reverse bias 20. This current remained nearly constant up to the reverse bias of ten volts 22. Even at forty volts, the dark reverse leakage current was only about 1.5 nA 26.

Using a calibrated UV-enhanced silicon photodiode, the responsivity for the transparent Schottky detector was measured. A Helium-Cadmium (He-Cd) laser at about 325 nm wavelength was used for these measurements. The

responsivity at reverse biases between approximately -5 and -10 V was about 0.19 Amps/Watt (A/W). As expected, the gain at reverse bias condition was nearly 1. However, at small forward biases, below the barrier turn-on voltage (0.7 V) 24, a high gain of approximately fifty was measured.

The low frequency noise for the transparent Schottky detectors was also measured. The major noise contribution was $1/f$-noise. At about 10 Hz, the noise spectral density was measured to be roughly 5 x 10^{-23} A^2/Hz. This noise level is about two orders of magnitude better than other GaN transparent Schottky devices with a mesa etch. The noise reduction may be attributed to the reduced leakage of the device.

The SiO_2 layers employed in the current invention are beneficial in developing GaN-based Field Effect Transistors.

In a second embodiment of the current invention, an AlGaN/GaN MOSHFET with a high-quality SiO_2/AlGaN interface on a sapphire substrate is presented. The device has output characteristics similar to an AlGaN/GaN HFET, however, the introduction of SiO_2 reduces the gate leakage by approximately six orders of magnitude, which is extremely important for high-power and low noise applications.

Figure 3 shows one embodiment of the present device structure. The AlGaN/GaN heterostructure was grown by MOCVD on a sapphire substrate 30. A roughly 50 nm AlN buffer layer (not shown) was first grown on the substrate 30. The next step was to apply the active layer. This included the deposition of an approximately 1 μm insulating GaN layer 32 and a roughly 50 nm n-GaN layer

(not shown) with an estimated doping level between $2x10^{17}$ cm^{-3} and $5x10^{17}$ cm^{-3}. Next, a barrier layer was applied. In this case, the heterostructures were capped with a roughly 30 nm $Al_{0.2}Ga_{0.8}N$ barrier layer 34, which was doped with silicon to approximately 2 x 10^{18} cm^{-3}. The measured Hall mobility was about 1,180 cm^2/V-s and the sheet carrier concentration was about 1.15 x 10^{13} cm^{-2}. Finally, prior to transistor fabrication, a roughly 15 nm SiO_2 layer 36 was applied onto the heterostructures using PECVD. The thickness was verified with capacitance-voltage (C-V) measurements on device wafers with and without the SiO_2 layer 36.

For fabricating the ohmic contact, the SiO_2 layer 36 was removed from the source 38 and drain 40 regions with buffered hydrofluoric (HF) solution. E-beam deposited Ti/Al/Ti/Au (~100 Å /~300 Å /~200 Å /~1000 Å) layers were used for Ohmic drain and source contacts. These contacts were annealed at about 850° C for about one minute using Rapid Thermal Anneal. The transistors had a source-drain spacing of roughly 5 μm, a gate length of roughly 2 μm, and a gate width of about 150 μm. Helium ion implantation was used to isolate devices. The Transmission Line Model (TLM) measurements yielded a specific contact resistance of about 8.5 x 10^{-6} Ωcm^2, a contact resistance of about 0.95 Ωmm, and a channel resistance of roughly 2.7 Ωmm. Using Ni/Au (~300 Å /~500 Å) for the gate metal, two sets of devices were then fabricated on the same wafer. These devices consisted of the structures with the gate metal 42 on top of the SiO_2 layer (MOSFET) and with the gate metal directly on the AlGaN barrier layer (not shown, base-line HFET).

In Figure 4, C-V plots for a base-line AlGaN/GaN HFET (dotted line) and a GaN/AlGaN-based MOSFET are shown. From the capacitance ratio of equal area contacts, the SiO_2 layer is estimated to be 13 nm thick. This is close to the value extracted from the PECVD growth rate.

Figure 5a shows the measured current-voltage (I-V) characteristics of the base-line HFET, while Figure 5b shows the measured I-V characteristics of the MOSFET fabricated under identical conditions. The device dimensions are exactly the same, except for the distance between the gate and the channel, which is greater for the MOSFET because of the additional approximately 15 nm SiO_2 layer.

As shown in Figure 5a, the maximum device current for the base-line HFET 50 (about 600 mA/mm) is comparable to the maximum device current for the MOSFET 52, shown in Figure 5b. The real space transfer into three-dimensional electronic states in GaN at high electron sheet carrier concentrations may limit the peak current in both devices.

From the C-V plots of Figures 5a and 5b, the gate capacitance for the MOSFET (~2,900 pF/mm^2) and the baseline HFET (~1,400 pF/mm^2) were extracted. For a MOSFET gate voltage swing of about 8 V, this corresponds to a sheet electron concentration in the channel, $n_s = Cg\ V_{gt}/q$, close to $1.4 \times 10^{13}\ cm^{-2}$, and to an effective carrier velocity in the channel, $v_{eff} = I/(q\ n_s)$, of about 0.3×10^5 m/s, which is quite reasonable. (Here q is the electronic charge and I is the device current per unit gate width.) The estimated value of the sheet electron

concentration is in good agreement with the measured values from the Hall mobility data.

Figure 6a shows the device saturation current and transconductance in the saturation region for the MOSFET and base-line HFET. As seen in the figure, the maximum saturation current is approximately the same for the two devices.

Figure 6b shows the device saturation transconductance in the saturation region for the MOSFET and base-line HFET. The MOSFET saturation transconductance 60 is smaller than that for the base-line HFET 62. This decrease is consistent with the larger separation between the MOSFET channel and the gate contact and with the smaller gate capacitance caused by the low dielectric constant of SiO_2.

The increased gate-to-channel separation is also responsible for a more negative MOSFET threshold voltage. The maximum transconductance 60, g_m = 75 mS/mm, was measured for a roughly 2 μm long gate device. However, as can be seen from Figure 6b, the MOSFET has an advantage of having a larger gate voltage swing and a higher linearity than the base-line HFET. This should lead to smaller intermodulation distortion, a smaller phase noise and a larger dynamic range compared to the HFET.

In Figure 7, the gate leakage current is shown as a function of voltage. The gate leakage currents for the MOSFET 70 and the base-line HFET 72 with identical device geometries are presented. The data demonstrate that the MOSFET leakage current is several orders of magnitude smaller than that for the

base-line HFET. This is advantageous for using the MOSFET as a microwave device.

Figure 8 shows the MOSFET gate leakage current as a function of temperature. The data shows that the MOSFET gate leakage current remains very low even at elevated temperatures up to about 600 degrees Kelvin 80. The activation energy depends on bias, and can be deduced from the slope of the dependence shown in Figure 8 in a conventional way. As can be seen, the leakage current is thermally activated with the activation energy at about 35 V on the order of 0.6 eV. This is consistent with the gate leakage current for thermionic-field emission mechanisms at large negative gate biases.

MOSHFETs may be beneficial for various high-power applications. These applications, however, place severe constraints on device thermal management, which can be hardly satisfied with low thermal conductivity sapphire substrates. Hence, AlGaN/GaN MOSHFETs were also developed over insulating 4H-SiC substrates. Device I-V curves demonstrate the channel current as high as about 1.3 A/mm without any evidence of current clamp or negative slope. The microwave and high temperature performance of these MOSHFETs are quite comparable to the base-line HFETs.

The device epilayer structure was grown by low-pressure MOCVD on insulating 4H-SiC substrates. All AlGaN/GaN layers for this structure were deposited at roughly 1000° C and 76 Torr. An approximately 50 nm AlN buffer layer was first grown at a temperature of about 1000° C, followed by the

deposition of an approximately 0.4 μm insulating GaN layer and a roughly 50 nm n-GaN layer with an estimated doping level between about 2 x 10^{17} cm^{-3} and 5 x 10^{17} cm^{-3}. The heterostructures were capped with a roughly 30 nm $Al_{0.2}Ga_{0.8}N$ barrier layer, which was doped with silicon to approximately 2 x 10^{18} cm^{-3}. An extremely low-level flux of trimethylindium (TMI) was also present during the growth of all the layers of the structure. The presence of the indium surfactant may assist in improving the surface and interface roughness through the incorporation of trace amounts of indium. The measured room temperature Hall mobility was about 1,150 cm^2/V-s and the sheet carrier concentration was roughly 1.2×10^{13} cm^{-2}.

Prior to transistor fabrication, an approximately 10 nm SiO_2 layer was deposited on part of the heterostructure using PECVD. The thickness of this layer, d_{OX}, was extracted from the capacitance-voltage (C-V) measurement at about 1 MHz on areas with and without the SiO_2 layer. From the zero volt capacitance of these metal-semiconductor structures (without SiO_2 layer), and using AlGaN layer permittivity $\varepsilon_B = 8.8$, the AlGaN barrier thickness, d_B, is estimated to be 31 nm. This is close to the 30 nm value estimated from the deposition rate. The oxide thickness, d_{OX}, was determined using the following equation:

$$C_{MOS} = C_{MS} * \left(\frac{1}{1 + \frac{d_{OX}}{d_B} \cdot \frac{\varepsilon_B}{\varepsilon_{OX}}} \right)$$

Here C_{MOS} and C_{MS} are the capacitances of equal area pads on the oxide and non-oxide areas and $\varepsilon_{OX} = 3.9$ is the SiO_2 dielectric permittivity. Using the data of the above equation, the SiO_2 thickness, d_{OX}, was estimated to be 7 nm. This is in reasonable agreement with the d_{OX} value of 10 nm expected from the deposition rate.

The C-V characteristics were also measured under a strong white light illumination. For the HFET structure (without the SiO_2 layer), the C-V curves in light and dark practically coincide. However, for the MOSHFET structure a threshold voltage shift $\Delta V \sim 1$ V is measured. This voltage shift is likely to be attributed to the charge $\Delta Q = C\,\Delta V$ induced near the SiO_2/AlGaN interface.

Using the MOSHFET device capacitance measured at $V \approx -9$ V, the surface charge density in SiO_2 layer, n_s, is estimated to be about 1×10^{12} cm^{-2}. This is one order of magnitude less than the sheet carrier density (of free carriers) in the 2D electron gas channel of the MOSHFET, thereby indicating a high quality for the SiO_2/AlGaN interface.

The use of SiO_2/AlGaInN or SiO_2/AlGaN structures allows for the development of a large periphery MG MOSHFET device using a unique oxide-bridging approach for source interconnections. This MG MOSHFET (fabricated on a SiC substrate) demonstrates a nearly linear dependence of saturation current, transconductance, microwave gain and saturation power on total device width in a range from about 0.15 to 4 mm. Saturation current, up to roughly 5.1 A was measured for a MOSHFET device with an approximately 6 mm wide gate.

Figure 9 shows an SEM image that displays the MG MOSHFET design. Multi gate device geometry consists of an interlaced source-gate-drain electrode structure. The source-to-source connections go over the gate electrodes with an oxide layer in between for isolation. First, Ohmic contacts for source and drain were fabricated using Ti (~200 Å)/Al (~500 Å)/Ti (~200 Å)/Au (~1500 Å). These were annealed at around 850° C for about 1 minute in nitrogen ambient. Prior to the gate fabrication, an approximately 10 nm SiO_2 layer was deposited on part of the heterostructure using plasma enhanced chemical vapor deposition (PECVD). Ni (~200 Å)/Au (~1000 Å) gate electrodes were then deposited in between the source-drain electrodes with and without SiO_2. A single gate electrode had a length of about 1.5 mm and width of roughly 250 μm. Prior to contact pad formation, PECVD was again used to deposit approximately 0.3 μm thick SiO_2 isolation "islands" at the gate - source intersections. Ti (~200 Å)/Au (~6000 Å) metal electrodes were then deposited to form low resistance section interconnections and device contact pads. The SiO_2 bridges (isolation pads) are estimated to increase the total device capacitance by less than 6% for this device symmetry. BCl_3 etched mesas were used for device-to-device isolation.

The current-voltage characteristics of a single section for the MOSHFET (~250 μm gate width) show the saturation current to be about 0.6 A/mm at zero gate bias. It increases to roughly 0.86 A/mm at a positive gate bias $V_g = +3$ V. The pinch-off voltage was about 9 V for MOSHFETs and about 5 V for the HFET devices fabricated on the same wafer. This difference is due to a larger gate-to-channel separation in the MOSHFET.

Figure 10 shows the saturation current as a function of total gate width. For both the HFET and MOSHFET devices, DC and pulsed saturation currents are shown. For these I-V measurements, the gate voltage was kept at about +3 V for MOSHFET and 0 V for the HFET (on the same wafer). As seen in the figure, the DC peak current for both device types saturates as the device periphery increases. However, pulsed I-Vs show nearly linear scaling. In pulsed I-V measurements, a saturation current as high as roughly 5.1 A was achieved for an approximately 6 mm wide MOSHFET device 100.

A similar design (but with a large drain-to-gate spacing) can be used for a power switching device. Figure 11 shows current as a function of voltage for such an MG MOSHFET switch. The maximum peak current value was more than 15 A/mm^2 while the gate leakage current was less than 1 nA/mm.

Figure 12 shows the MOSHFET breakdown voltage as a function of the gate-to-drain separation. For comparison, the figure also shows the breakdown voltage for an identical geometry HFET fabricated on the same wafer. Both devices show almost linear dependence of breakdown voltage on gate-to-drain distance reaching about 500 V at roughly 10 μm spacing. Thus, the maximum switching power of the device is about 7.5 kW/mm^2. Note that for these estimations, the total device area was used including the roughly 100 μm separation between adjacent gate sections. Using only the active source-drain region area, the switched power density estimate increases to about 50 kW/mm^2.

The specific on-state resistance of the drift region of the MOSHFET switch is less than about 75 mOhm-mm^2, which is 2 - 3 times less than that

reported for buried channel SiC FETs and 25 - 100 times less than that for induced channel SiC MOSFET switches.

Although the GaN-AlGaN MOSHFET is a normally-on device, its input current is extremely small. Even at an elevated temperature of about 250° C, the MOSHFET gate leakage current was measured to be roughly 0.5 nA. Furthermore, a MOSHFET can be converted into a normally-off device by adjusting the thickness of the AlGaN barrier layer and the residual doping in the GaN channel. This performance can also be compared with the switching SiC diode characteristics. This comparison shows that the three-terminal MOSHFET switch performs as well as the best SiC diodes.

The pulse response for a single approximately 250 micron section of the MG MOSHFET switch was measured. The voltage pulse was measured across a roughly 10 Ohm load resistor connected in series with the drain. The DC drain bias and gate-offset voltages were kept at about 15 V and -10 V respectively. The current in the "off state" of the switch was less than about 10 $\mu A/mm^2$. The "on state" current at about +3 V gate bias reaches approximately 11.2 A/mm^2 which is quite close to the steady state value at the same bias, showing no current collapse in the pulsed operation. The current pulse rise time of about 5 ns was limited by the input pulse rise time from the pulse generator.

The foregoing description of the preferred embodiments of this invention has been presented for purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form disclosed, and obviously, many modifications and variations are possible. Such modifications

and variations that may be apparent to a person skilled in the art are intended to be included within the scope of this invention as defined by the accompanying claims.